

FIG. 1

2 / 6

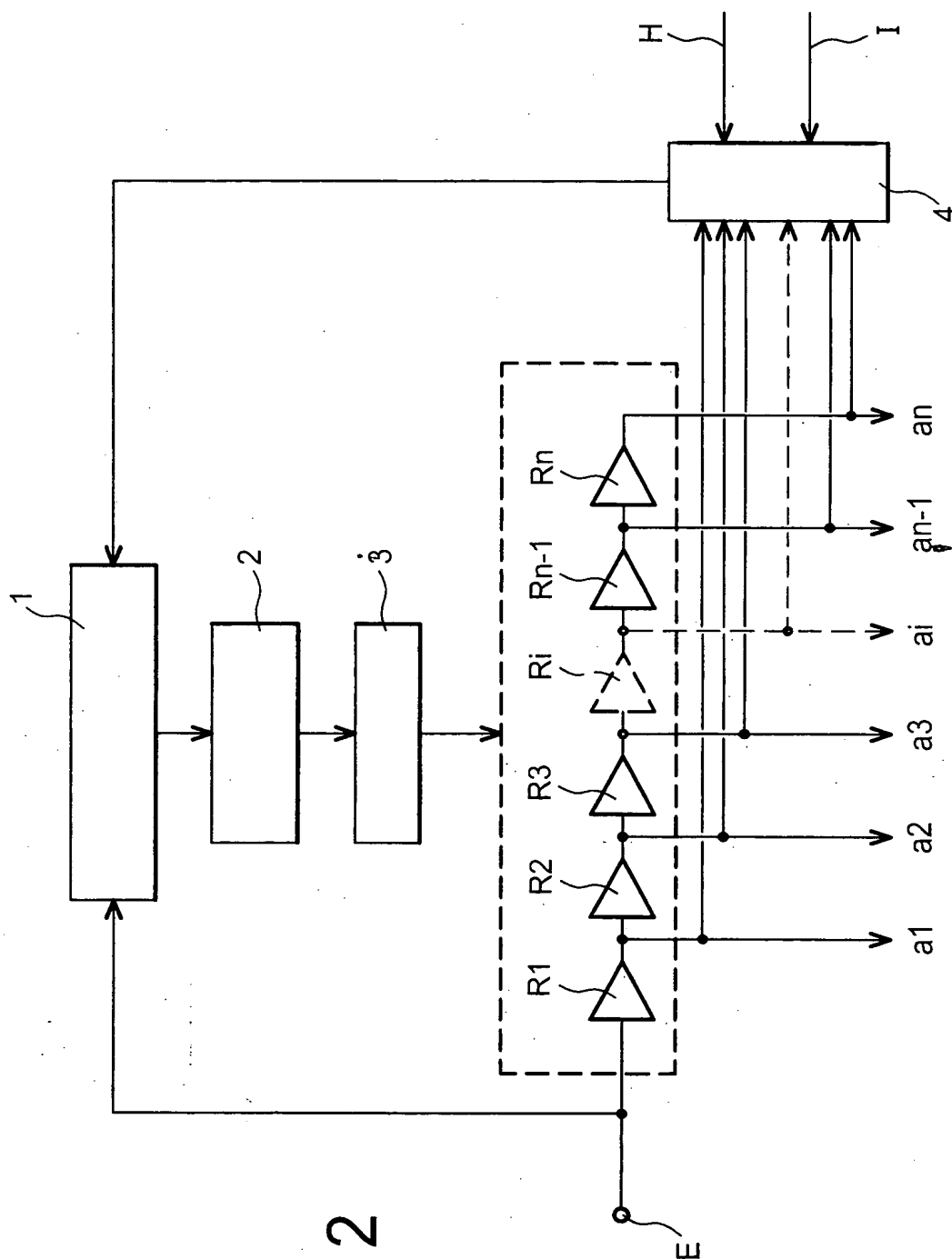


FIG. 2

FIG. 3

FIG. 3 is a block diagram of a digital filter circuit. The circuit includes a feedback loop starting from a terminal 'E' that passes through a series of blocks labeled 1, 2, and 3. The output of block 3 is fed into a multi-input summing junction (block 6, labeled $\Sigma\Delta$). This junction also receives inputs from a set of delay elements ($R_1, R_2, R_3, R_i, R_{n-1}, R_n$) and a direct input 'I'. The output of the summing junction is fed into a multi-input multiplier (block 5). The multiplier's output is fed back to the input of block 1. The multiplier also receives inputs from a set of multipliers ($R_1, R_2, R_3, R_i, R_{n-1}, R_n$) and a direct input 'C'. The multipliers are connected to a set of inputs labeled $a_1, a_2, a_3, a_i, a_{n-1},$ and a_n . The entire circuit is enclosed in a dashed box labeled 4.

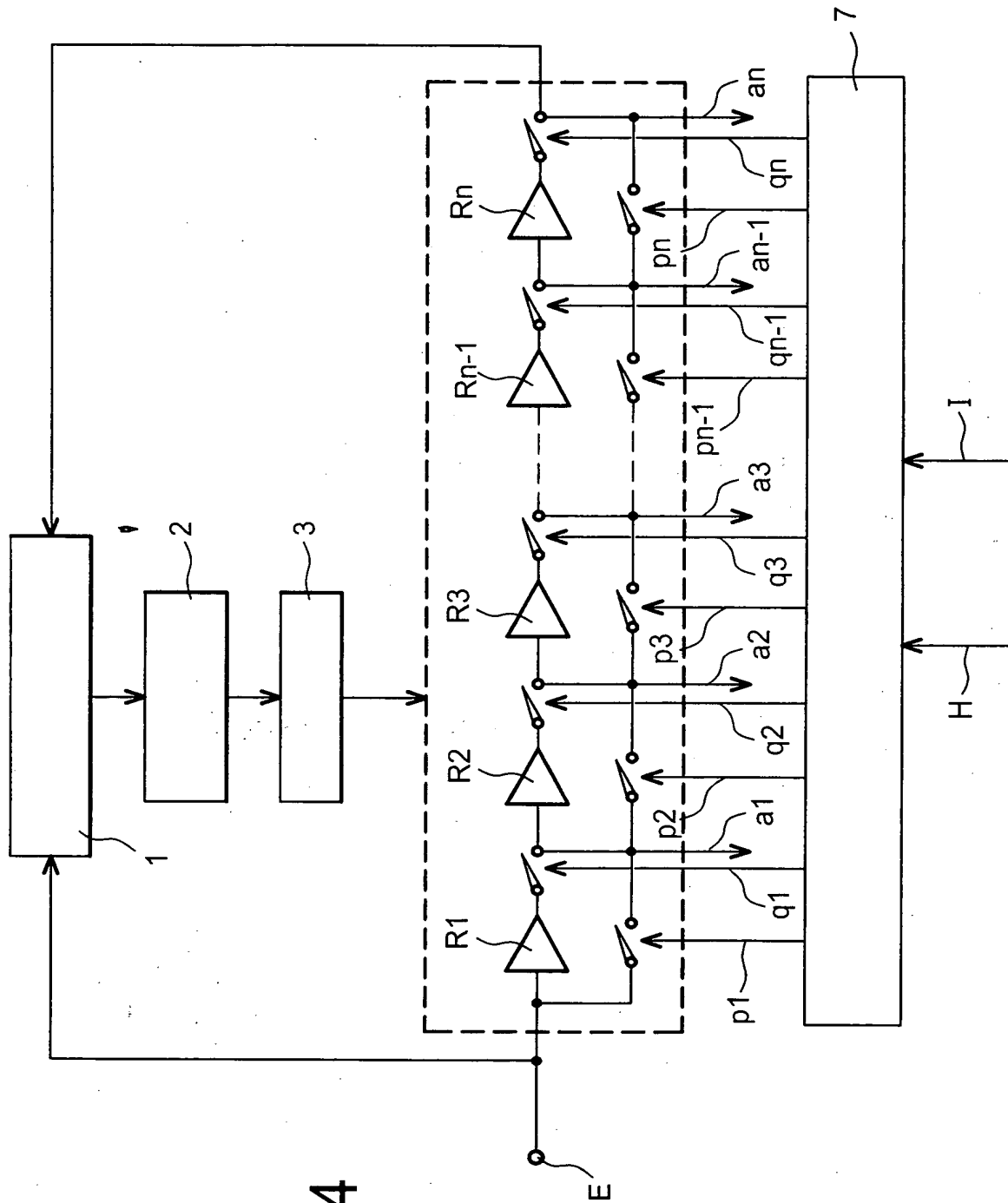
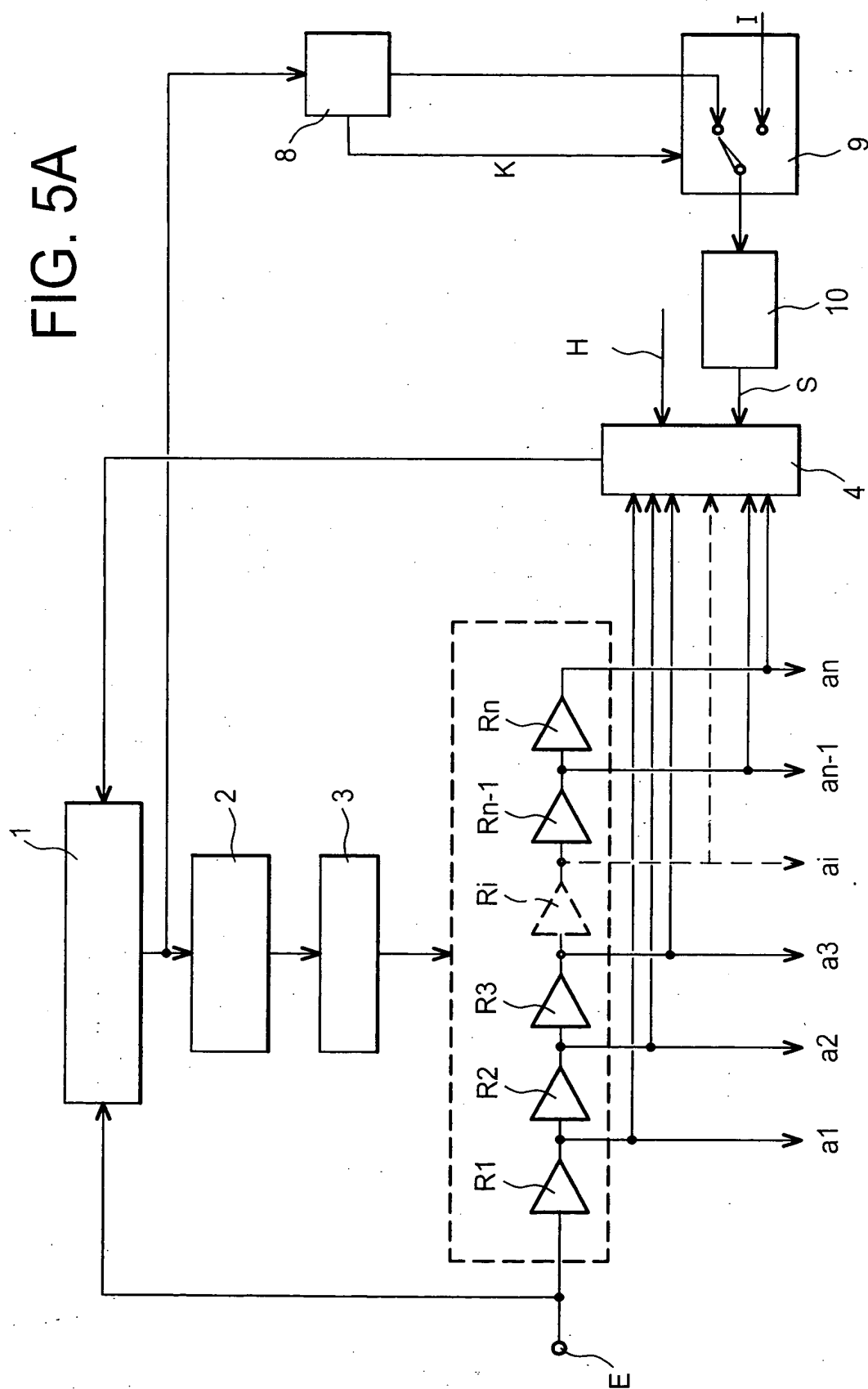


FIG. 4



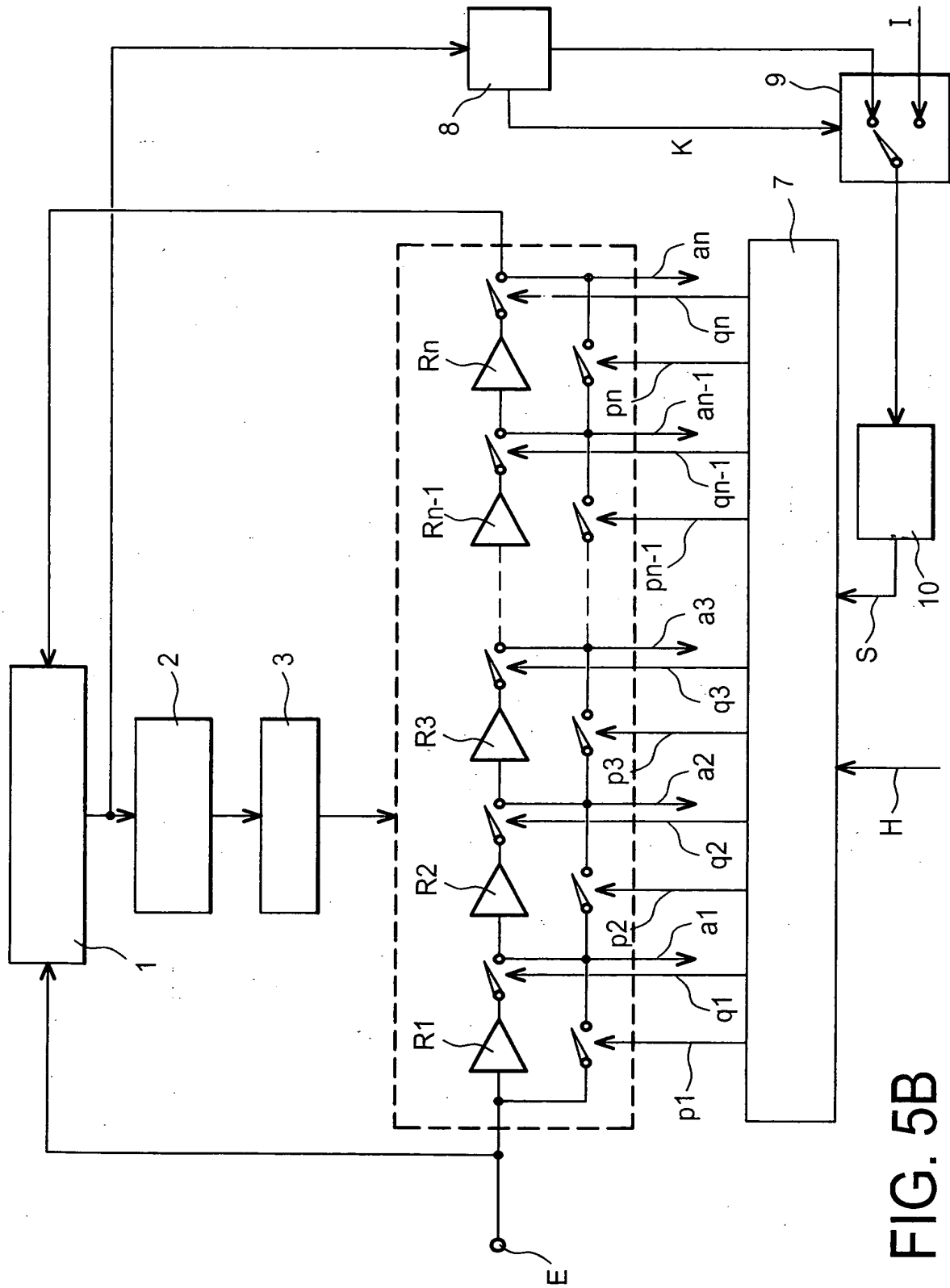


FIG. 5B